

ViaSat's ECC66100 is a family of soft decision Forward Error Correction (FEC) IP cores based on turbo product code (TPC) designed for use in 100 Gbps communications applications.

TPCs are the optimum FEC for high data rate applications as they provide high NECG (Net Electrical Coding Gain) with low implementation complexity. TPCs also have large minimum distances leading to a very low error floor, several orders of magnitude below the target $1e-15$ BER (Bit Error Rate), based on Asymptotic analysis.

ECC66100's underlying TPC architecture has been used extensively for a variety of applications that has proven successful in both simulations and hardware.

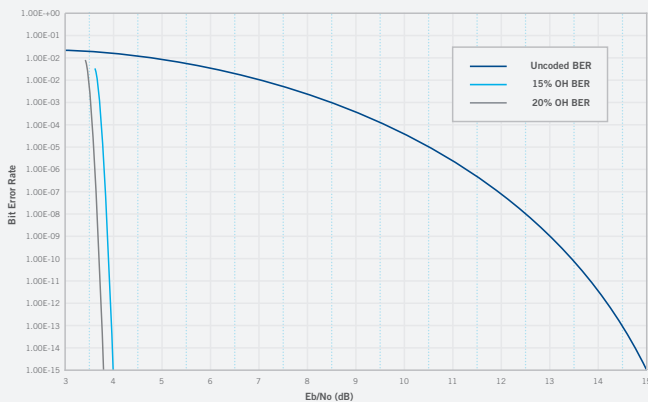
The ECC66100 series consists of the following overhead rates:

- » 15% with 11dB NECG
- » 20% with 11.3dB NECG

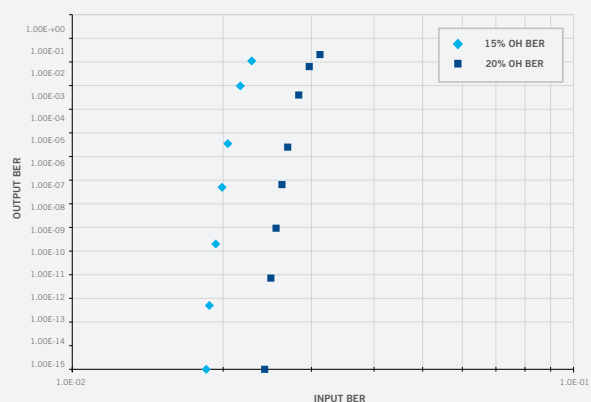
SOFT DECISION FEC

Encoder and decoder features:

- » 100G OTU4 application
- » 15% or 20% overhead rate
- » NECG of 11 or 11.3 dB
- » High burst error correction
- » Extensively proven TPC core architecture
- » Low implementation complexity
- » Easily configurable to achieve desired performance and complexity
- » Low latency



SOFT DECISION FEC PERFORMANCE



OUTPUT BER VS. INPUT BER

SPECIFICATIONS

FEATURE/PARAMETER

Coded Line Rate 120 Gbps (15% OH) / 126 Gbps (20% OH)

NECG 11dB (15% OH) / 11.3dB (20% OH)

Clocking 500 MHz

Burst Error Correction 1536 (15% OH) / 1152 (20% OH)

Soft decision Resolution

- » 4 bits
- » LLR input 8 bits I & Q

Latency

- » Encoder: 2 μ s (15% OH), 1 μ s (20% OH)
- » Decoder: less than 8 μ s (15% OH), 5 μ s (20% OH)

Power Consumption 40 nm process <8 W Typ.

Size (Includes Flipflops, Logic Gates and RAM)

- » Encoder + interleaver 1.64 M Equivalent Gates (15/ 20% OH)
- » Decoder + deinterleaver 25.8 M Equivalent Gates (15% OH) / 22.0 M Equiv Gates (20% OH)

DELIVERABLES

- » Encrypted RTL: Synopsys and or Cadence compatible
- » System Verilog, VMM based testbench and testcases
- » 'C' SW model (gcc object file)
- » User documentation

RELATED VIASAT PRODUCTS

- » DSP IP cores for coherent receiver and transmitter
- » FPGA demonstration platform for algorithm verification

Visit www.viasat.com for further information

FIGURE 1. TPC DECODER

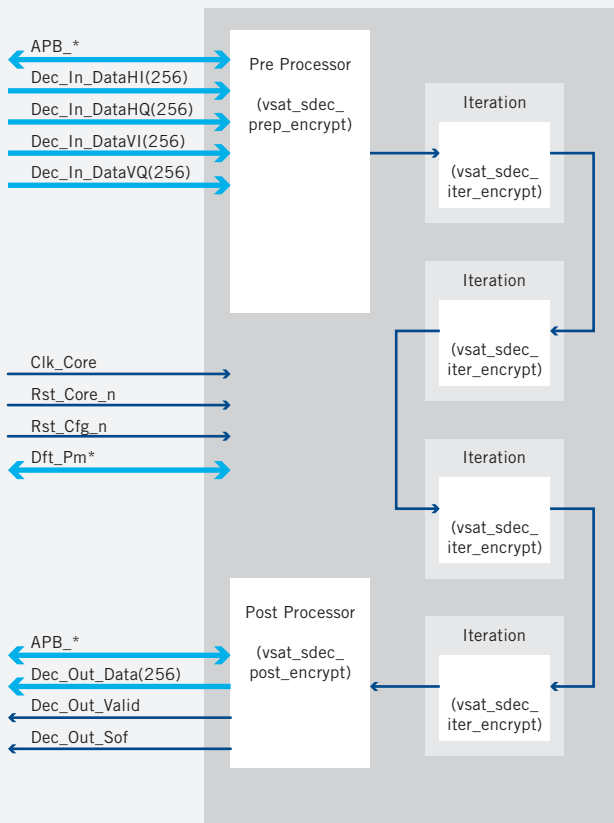
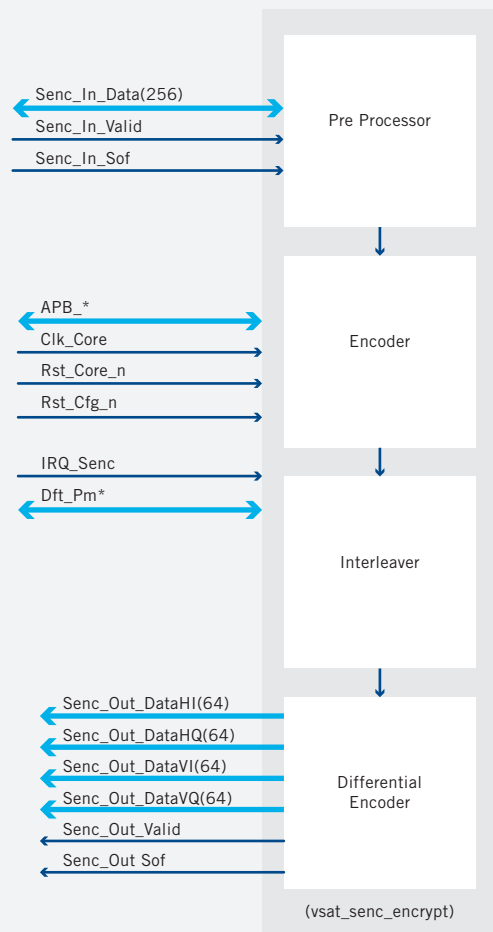


FIGURE 2. TPC ENCODER



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