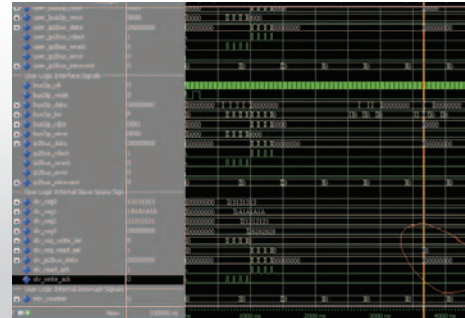


ViaSat IP cores enable 100 Gbps optical communications and beyond.



ViaSat specializes in forward error correction (FEC), signal processing, and hardware platforms. Our communications expertise has evolved from working with extreme channel conditions and impairments in satellite systems. 100 Gbps signals traveling through optical fibers face similar challenges due to channel impairments and the resulting signal degradation.

We have developed and implemented proven FEC modules that are necessary to achieve 100 Gbps throughput. FEC technologies include high gain turbo product code (TPC), low density parity check (LDPC), and Bose-Chaudhuri-Hocquenghem (BCH). Our products include IP cores for FPGAs and ASICs.

ADVANCED FEC DESIGNS IMPROVE DISTANCE/CAPACITY

Advanced FEC increases the effective optical signal-to-noise ratio (OSNR), providing additional optical link-margin and increasing these distance/capacity parameters:

- » Number of transmitted wavelengths (WDM channels)
- » Maximum distance for each transmitted signal
- » Bit rate of the optical channel

Our soft- and hard-decision FECs exceed the ITU-T G.709 and G.975 submarine standards for long haul (LH) and ultra-long haul (ULH) link performance requirements.

FPGA AND ASIC CORES

Product Number	Code Type	Approximate Overhead %	NECG (dB) for 1e-15 BER
ECC66100.HD7	TPC Hard-decision	7	9.3
ECC66100.SD7	TPC Soft-decision	7	10.3
ECC66100.HD15	TPC Hard-decision	15	9.8
ECC66100.SD15	TPC Soft-decision	15	11.1
ECC66100.SD20	TPC Soft-decision	20	11.4

Data rates up to 100 Gbps. Higher rates under development.

Customization includes other overhead rates, block sizes, and latency.

CUSTOM PRODUCTS

- » FECs for proprietary systems
- » Modulators and demodulators (DQPSK, QPSK, 8PSK, n-QAM, OFDM)
- » Digital signal processing

Additional services include engineering, consulting, and trade studies that define and create a communication system that meets your requirements.

Our ASIC technologies span 150 nm down to 40 nm using NEC, Fujitsu, IBM, and Honeywell processes. We are equipped with Synopsys, Cadence, and Mentor Graphics tools that support each ASIC design value chain segment, and Linux-based servers for our ASIC simulation environment.

ViaSat design architects and engineers are ready to provide you with exceptional customer service for design, verification, and back-end support.



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